Abstract of the Disclosure

In a method for forming a semiconductor device and a semiconductor device having an overlay mark, a first pattern for the semiconductor device is formed in a semiconductor device formation region of a semiconductor substrate and simultaneously in a first mark formation region of the semiconductor substrate. A second pattern for the semiconductor device is formed on a resultant structure in the semiconductor device formation region of the semiconductor substrate and simultaneously in a second mark formation region of the semiconductor substrate. The first and second patterns in the first and second mark formation regions, respectively, are inspected for misalignments using overlay marks formed to have shapes and sizes identical to those of real patterns in the semiconductor device formation region of the semiconductor substrate. By measuring misalignments of real patterns using the overlay marks, overlay mismatch between the semiconductor device formation region and the overlay mark may be prevented.